ISOLATED DC-DC CONVERTER

CFDHR500 SERIES

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Contents

Model Number	Input Voltage	Output Voltage	Output Current		Input Current		% EFF.		Capacitive Load Max.
			Min.	Max.	No Load	Full Load	(2)	(3)	
CFDHR500-24S12	9-40VDC	12VDC	0mA	42A	80mA	22.4A	91	91	42000uF
CFDHR500-24S24		24VDC	0mA	21A	80mA	22.4A	91	90	21000uF
CFDHR500-24S28		28VDC	0mA	18A	80mA	22.4A	91	90	18000uF
CFDHR500-24S54		54VDC	0mA	9.26A	100mA	22.4A	91	90	4000uF

1. Introduction

The CFDHR500-24SXX series of DC-DC converters offers 500 watts of output power @ single output voltages of 12, 24,28,48,54VDC with industry standard quarter-brick. It has a 4:1 input voltage range of 9 to 40VDC (24VDC nominal) and 3000VDC Basic isolation.

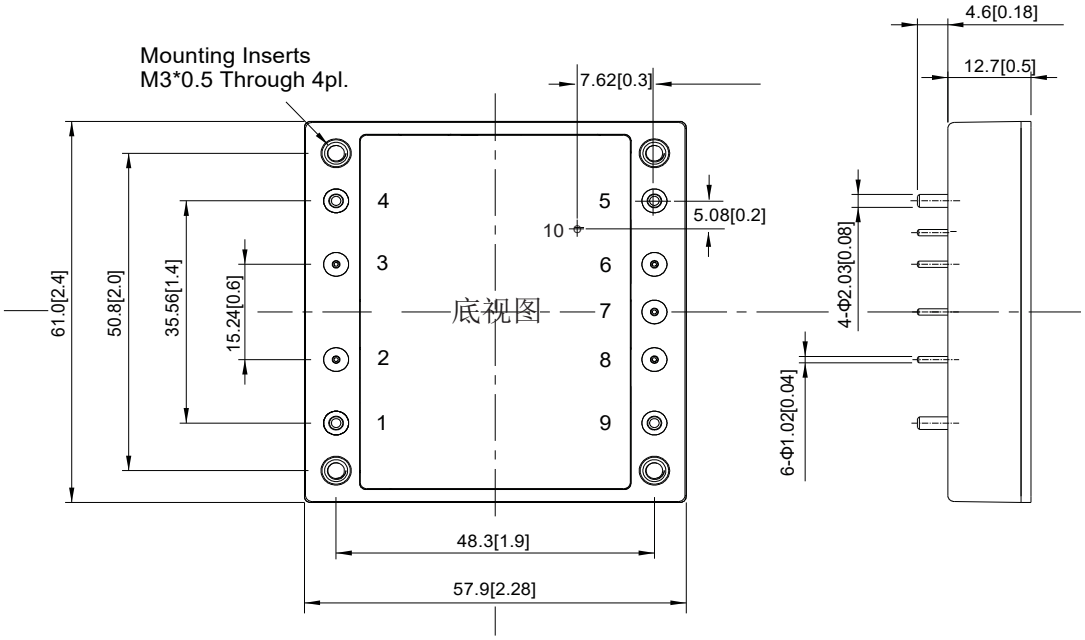
Compliant with EN55032. High efficiency up to 91.5%, allowing case operating temperature range of -40℃ to 105℃. An optional heat sink is available to extend the full power range of the unit.

The standard control functions include remote on/off (positive or negative) and +15% to -20% (except for 54Vout +10% to -20%) adjustable output voltage.

Fully protected against input UVLO (under voltage lock out),output over-current,output over-voltage,over-temperature and continuous short circuit conditions.

CFDHR500-24SXX series is designed primarily for common applications of 12V,24V nominal voltage and also suitable for distributed power architectures, telecommunications,battery operated equipment and industrial applications.

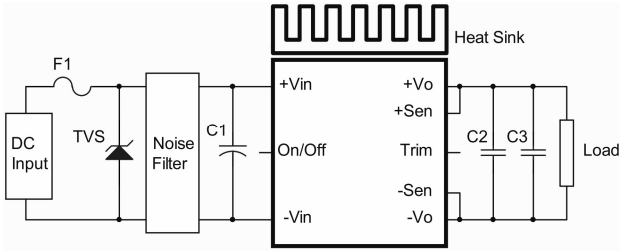
2. Pin Function Description



Pin	Function
1	+Vin
2	On/Off
3	CASE
4	-Vin
5	-Vo
6	-Sense
7	Trim
8	+Sense
9	+Vo
10	PC

3. Connection for Standard Use

The connection for standard use is shown below.An external input capacitor (C1) 2200uF for all models is recommended to reduce input ripple voltage.External output capacitors (C2,C3) are recommended to reduce output ripple and noise,10uF polymer tantalum and 1uF ceramic capacitors for all models.



Symbol	Component	Reference
F1, TVS	Input fuse, TVS	Section 1 0.1
C1	External capacitor on the input side	Note Section 7.2
C2,C3	External capacitor on the output side	Section 7.3/7.4
Noise Filter	External input noise filter	Section 10.2
Remote On/Off	External Remote On/Off control	Section 6.5
Trim	External output voltage adjustment	Section 6.7
Heat sink	External heat sink	Section 9.2/9.3/9.4/9.5
+Sense/-Sense	--	Section 6.6

Note:
If the impedance of input line is high, C1 capacitance must be more than above. Use more than two recommended capacitors above in parallel when ambient temperature becomes lower than -20℃.

4. Test Set-Up

The basic test set-up to measure parameters such as efficiency and load regulation is shown below. When testing the modules under any transient conditions please ensure that the transient response of the source is sufficient to power the equipment under test. We can calculate:

Efficiency
Load regulation and line regulation.

The value of efficiency is defined as:

$$\eta = \frac{V_o \times I_o}{V_{in} \times I_{in}} \times 100\%$$

Where:

V_o is output voltage,
I_o is output current,
V_{in} is input voltage,
I_{in} is input current.

The value of load regulation is defined as:

$$Load\ reg. = \frac{V_{FL} - V_{NL}}{V_{NL}} \times 100\%$$

Where:

V_{FL} is the output voltage at full load.
V_{NL} is the output voltage at no load.

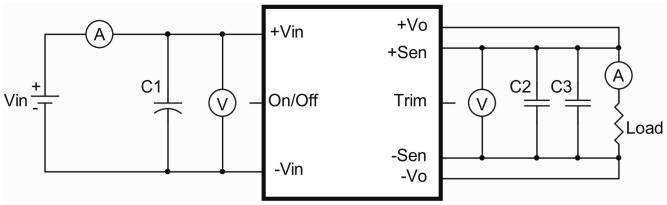
The value of line regulation is defined as:

$$Line\ reg. = \frac{V_{HL} - V_{LL}}{V_{LL}} \times 100\%$$

Where:

V_{HL} is the output voltage of maximum input voltage at full load.

V_{LL} is the output voltage of minimum input voltage at 80% full load.

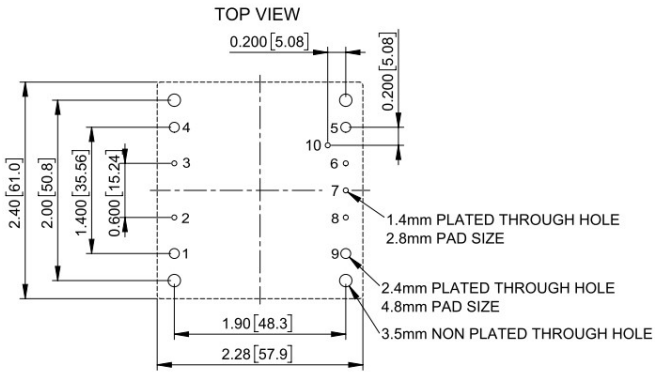


CFDHR500-24SXX Series Test Setup

C1:2200uF/63V ESR<0.056Ω
C2:1uF/1210 ceramic capacitor
C3:10uF polymer tantalum capacitor (ESR ≦0.05Ω)

5. Recommend Layout, PCB Footprint and Soldering Information

The system designer or end user must ensure that metal and other components in the vicinity of the converter meet the spacing requirements for which the system is approved.Low resistance and inductance PCB layout traces are the norm and should be used where possible. Due consideration must also be given to proper low impedance tracks between power module,input and output grounds.

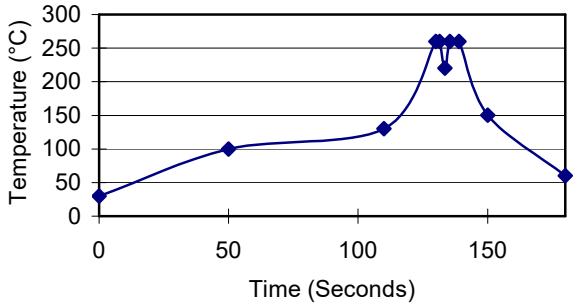


Option Module

Clean the soldered side of the module with a brush, prevent liquid from getting into the module. Do not clean by soaking the module into liquid. Do not allow solvent to come in contact with product labels or resin case as this may changed the color of the resin case or cause deletion of the letters printed on the product label. After cleaning, dry the modules well.

The suggested soldering iron is 450℃ for up to 5 seconds (less than 50W). Furthermore, the recommended soldering profile is shown below,and PCB layout is referring to Section 10.2.

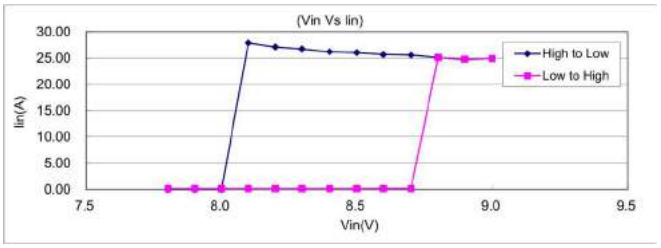
Lead Free Wave Soldering Profile



6. Features and Functions

6.1 UVLO (Under Voltage Lock Out)

Input under voltage lockout is standard on the CFDHR500-24SXX series unit.The unit will shut down when the input voltage drops below a threshold, and the unit will operate when the input voltage goes above the upper threshold.

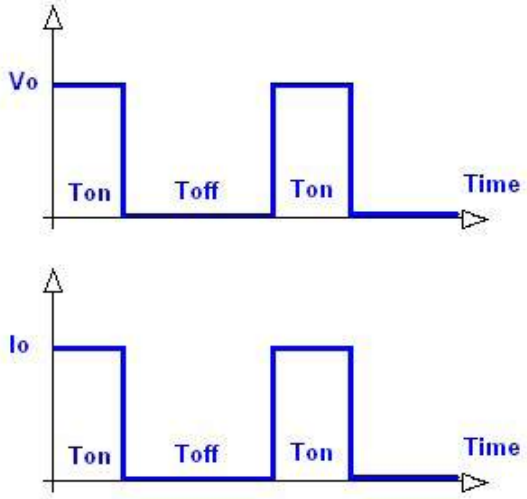


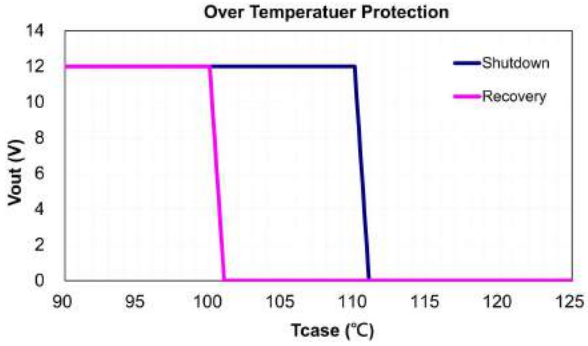
Note:

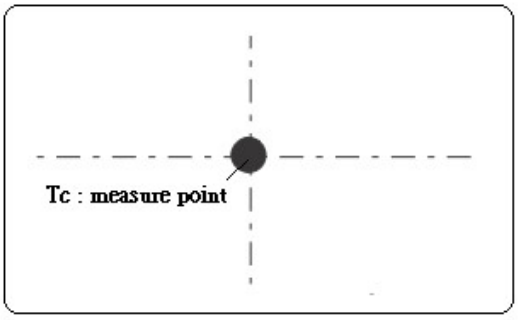
If need to configure UVLO turn off threshold to 8V$_{DC}$, please make sure the output power is no more than 80% full load, even though the 9V operating is short duration. And the module operating between input 9Vdc to 12V$_{DC}$, please make sure the output power is no more than 80% full load.

6.2 Over Current/Short Circuit Protection

All models have internal over current and continuous short circuit protection. The unit operates normally once the fault condition is removed. At the point of current limit inception, the converter will go into hiccup mode protection.







6.3 Output Over Voltage Protection

The output over voltage protection consists of circuitry that internally limits the output voltage. If more accurate output over voltage protection is required, then an external circuit can be used via the remote on/off pin.

Note:

Please note that device inside the power supply might fail when voltage more than rate output voltage is applied to output pin. This could happen when the customer tests the over voltage protection of unit. OVP can be tested by using the TRIM UP function. Consult us for more information.

6.4 Over Temperature Protection

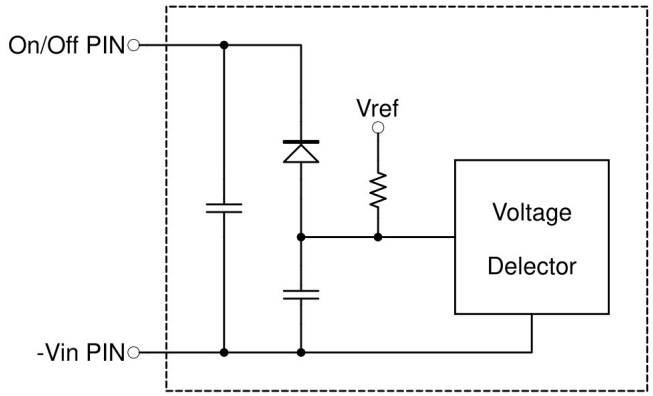
These modules have an over temperature protection circuit to safeguard against thermal damage. Shutdown occurs with the maximum case reference temperature is exceeded.The module will restart when the case temperature falls below over temperature recovery threshold.Please measure case temperature of the center part of aluminum base plate.

6.5 Remote On/Off

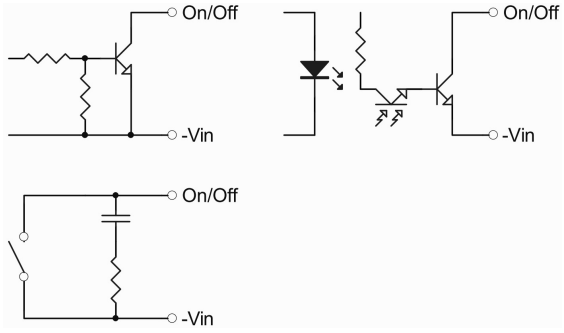
The CFDHR500-24SXX series allows the user to switch the module on and off electronically with the remote On/Off feature. All models are available in “positive logic” and “negative logic” (optional) versions. The converter turns on if the remote On/Off pin is high (>3.5V_{DC} to 65Vdc or open circuit). Setting the pin low (0 to<1.2V_{DC}) will turn the converter off. The signal level of the remote On/Off input is defined with respect to ground.
If not using the remote On/Off pin,leave the pin open (converter will be on).
Models with part number suffix “N” are the “negative logic” remote On/Off version. The unit turns off if the remote On/Off pin is high (>3.5Vdc to 65V_{DC} or open circuit). The converter turns on if the On/Off pin input is low (0 to<1.2V_{DC}).Note that the converter is off by default.

Logic State (Pin 2)	Negative Logic	Positive Logic
Logic Low	Module on	Module off
Logic High	Module off	Module on

The converter remote On/Off circuit built-in on input side. The ground pin of input side Remote On/Off circuit is -Vin pin. Inside connection sees below.



Connection examples see below.



Remote On/Off Connection Example

6.6 Output Remote Sensing

The CFDHR500-24SXX series converter has the capability to remotely sense both lines of its output. This feature moves the effective output voltage regulation point from the output of the unit to the point of connection of the remote sense pins. This feature automatically adjusts the real output voltage of the CFDHR500-24SXX series in order to compensate for voltage drops in distribution and maintain a regulated voltage at the point of load. The remote-sense voltage range is:

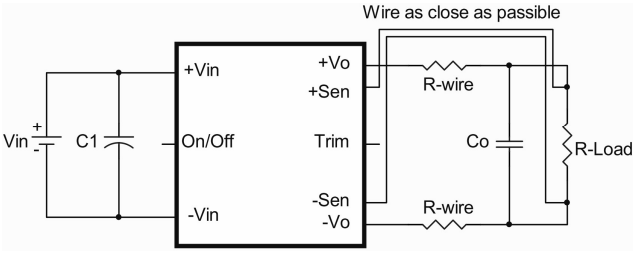
For Vo=54V

$[(+V_{out}) - (-V_{out})] - [(+Sense) - (-Sense)] \leqq 10\% \text{ of } V_{o\_nominal}$

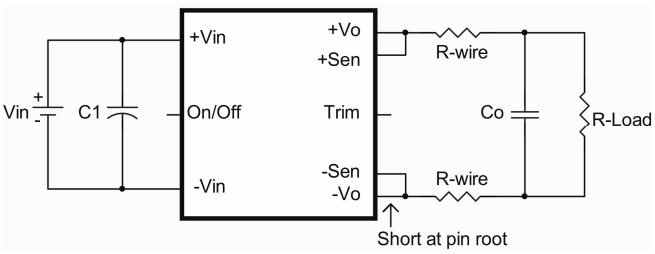
For Others

$[(+V_{out}) - (-V_{out})] - [(+Sense) - (-Sense)] \leqq 15\% \text{ of } V_{o\_nominal}$

When remote sense is in use, the sense should be connected by twisted-pair wire or shield wire.If the sensing patterns short,heave current flows and the pattern may be damaged. Output voltage might become unstable because impedance of wiring and load condition when length of wire is exceeding 400mm.This is shown in the schematic below.



If the remote sense feature is not to be used, the sense pins should be connected locally. The +Sense pin should be connected to the +Vout pin at the module and the -Sense pin should be connected to the -Vout pin at the module. Wire between +Sense and +Vout and between -Sense and -Vout as short as possible. Loop wiring should be avoided. The converter might become unstable by noise coming from poor wiring. This is shown in the schematic below

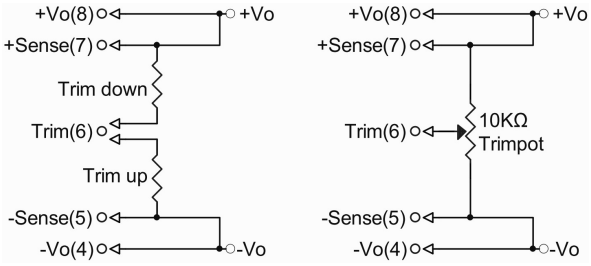


Note:

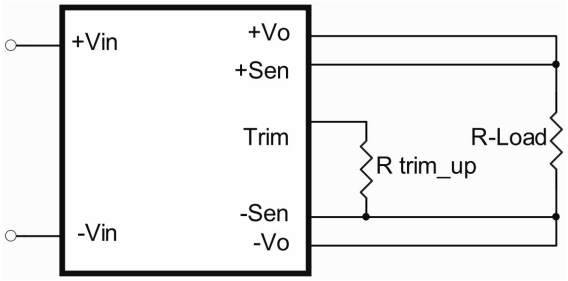
Although the output voltage can be varied (increased or decreased)by both remote sense and trim,the maximum variation for the output voltage is the larger of the two values not the sum of the values. The output power delivered by the module is defined as the voltage at the output terminals multiplied by the output current. Using remote sense and trim can cause the output voltage to increase and consequently increase the power output of the module if output current remains unchanged. Always ensure that the output power of the module remains at or below the maximum rated power. Also be aware that if $V_{o.set}$ is below nominal value, $P_{out.max}$ will also decrease accordingly because $I_{o.max}$ is an absolute limit. Thus, $P_{out.max} = V_{o.set} \times I_{o.max}$ is also an absolute limit.

6.7 Output Voltage Adjustment

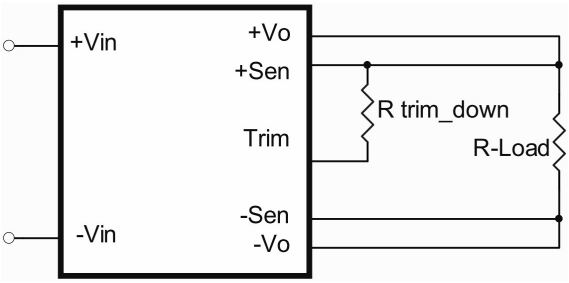
Output may be externally trimmed (+15% to -20%, except 54Vout is +10% to -20%) with a fixed resistor or an external trim pot as shown (optional). Model specific formulas for calculating trim resistors are available upon request as a separate document.



In order to trim the voltage up or down, one needs to connect the trim resistor either between the trim pin and -Sense for trim-up or between trim pin and +Sense for trim-down.The output voltage trim range is +15% to -20%, except 54Vout, it is +10% to -20%. This is shown:



Trim-up Voltage Setup



Trim-down Voltage Setup

The value of R $_{trim\_up}$ defined as:

$$R_{trim\_up} = \left[\frac{V_r \times R1 \times (R2 + R3)}{R2 \times (V_o - V_{o,nom})}\right] - Rt \ (K\Omega)$$

Where:

R_{trim_up} is the external resistor in KΩ.

$V_{o,\ nom}$ is the nominal output voltage.

V_o is the desired output voltage.

R1, R2, R3, Rt and Vr are internal to the unit and are defined in Table 1.

Table 1 – Trim up and Trim down Resistor Values

Model Number	Output Voltage(V)	R1 (KΩ)	R2 (KΩ)	R3 (KΩ)	Rt (KΩ)	Vr (V)
CFDHR500-24S12	12.0	6.8	2.37	2.2	10	2.5
CFDHR500-24S24	24.0	15	2.43	5.9	20	2.5
CFDHR500-24S28	28.0	15.4	2.49	10	23.2	2.5
CFDHR500-24S48	48.0	28.7	2.4	15	43.2	2.5
CFDHR500-24S54	54.0	36	2.43	14	51	2.5

For example,to trim-up the output voltage of 12V module (CFDHR500-24S12) by 15% to 13.8V,R_{trim_up} is calculated as follows:

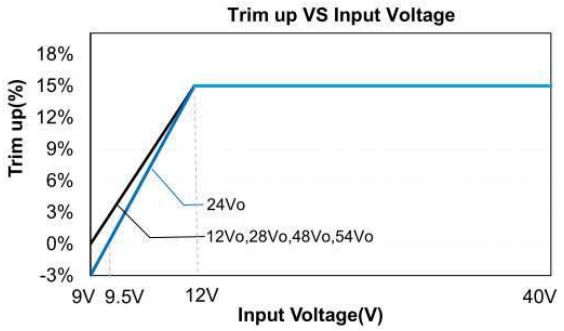
R1=6.8KΩ , R2=2.37KΩ , R3=2.2KΩ , Rt=10KΩ , Vr=2.5V, Vo=13.8V, Vo, nom=12V

$$R_{trim_{up}} = \left[\frac{2.5 \times 6.8 \times (2.37 + 2.2)}{2.37 \times (13.8 - 12)}\right] - 10 = 8.2 \ (K\Omega)$$

The typical value of R $_{trim\_up}$

Trim up (%)	12V	24V	28V	48V	54V
	R_{trim_up} (KΩ)				
1%	263.17	515.62	666.51	1040.5	1075
2%	126.59	247.81	321.65	498.72	512.44
3%	81.06	158.54	206.70	318.04	324.63
4%	58.29	113.91	149.23	227.73	230.72
5%	44.63	87.12	114.74	173.54	174.38
6%	35.53	69.27	91.75	137.42	136.81
7%	29.02	56.52	75.33	111.62	109.98
8%	24.15	46.95	63.01	92.27	89.86
9%	20.35	39.51	53.43	77.21	74.21
10%	17.32	33.56	45.77	65.17	61.69
11%	14.83	28.69	39.50	55.32	
12%	12.76	24.64	34.28	47.11	
13%	11.01	21.20	29.85	40.16	
14%	9.51	18.26	26.06	34.21	
15%	8.21	15.71	22.78	29.05	

CFDHR500-24SXX series has Trim up Derating by Input Voltage is required shown below.



The value of R_{trim_down} defined as:

$$R_{trim_{down}} =$$

$$R1 \times \left[\frac{V_r \times R1}{R2 \times (V_{o,nom} - V_o)} - 1 \right] - Rt \ (K\Omega)$$

Where:

R_{trim_down} is the external resistor in KΩ .

$V_{o,\ nom}$ is the nominal output voltage.

V_o is the desired output voltage.

R1, R2, R3, Rt and Vr are internal to the unit and are defined in Table 1.

For example: to trim-down the output voltage of 12V module (CFDHR500-24S12) by 20% to 9.6V, R_{trim_down} is calculated as follows:

R1=6.8KΩ , R2=2.37KΩ , R3=2.2KΩ , Rt=10KΩ , Vr=2.5V, Vo=9.6V, Vo, nom=12V

$$R_{trim_{down}} =$$

$$6.8 \times \left[\frac{2.5 \times 6.8}{2.37 \times (12 - 9.6)} - 1 \right] - 10 = 3.52 \ (K\Omega)$$

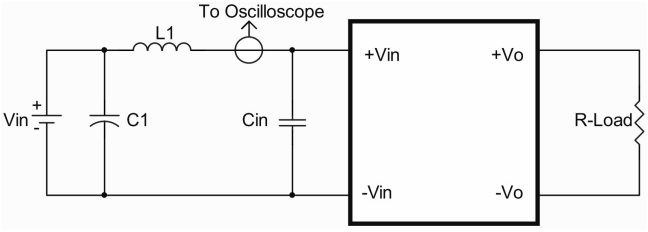
The typical value of R_{trim_down}

Trim down (%)	12V	24V	28V	48V	54V
	R_{trim_down} (KΩ)				
1%	389.67	929.51	811.80	1715.6	2382.1
2%	186.43	447.25	386.60	821.86	1147.5
3%	118.69	286.50	244.87	523.94	736.05
4%	84.82	206.13	174.00	374.98	530.28
5%	64.49	157.90	131.48	285.60	406.83
6%	50.94	125.75	103.13	226.02	324.52
7%	41.27	102.79	82.89	183.46	265.73
8%	34.01	85.56	67.70	151.54	221.64
9%	28.36	72.17	55.89	126.71	187.35
10%	23.85	61.45	46.44	106.85	159.91
11%	20.15	52.68	38.71	90.60	137.47
12%	17.07	45.38	32.27	77.06	118.76
13%	14.47	39.19	26.82	65.60	102.93
14%	12.23	33.89	22.14	55.78	89.37
15%	10.30	29.30	18.09	47.27	77.61
16%	8.60	25.28	14.55	39.82	67.32
17%	7.11	21.74	11.42	33.25	58.24
18%	5.78	18.58	8.64	27.41	50.17
19%	4.59	15.76	6.16	22.18	42.95
20%	3.52	13.23	3.92	17.48	36.46

7. Input/Output Considerations

7.1 Input Capacitance at the Power Module

The converters must be connected to low AC source impedance. To avoid problems with loop stability source inductance should be low. Also, the input capacitors (Cin) should be placed close to the converter input pins to de-couple distribution inductance. However, the external input capacitors are chosen for suitable ripple handling capability. Low ESR capacitors are good choice. Circuit as shown as below represents typical measurement methods for reflected ripple current. C1 and L1 simulate a typical DC source impedance. The input reflected-ripple current is measured by current probe to oscilloscope with a simulated source Inductance (L1).



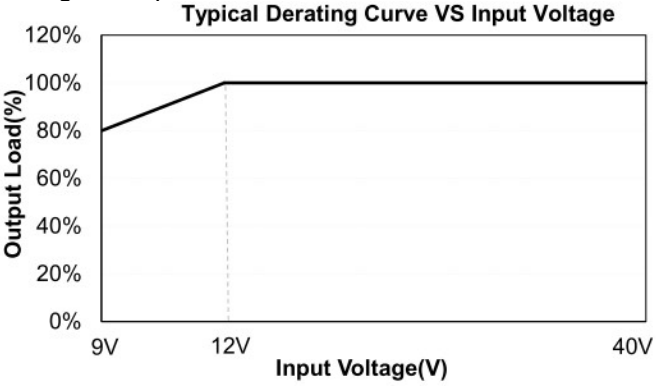
L1:3uH

C1:1000uF/100V (KMG) aluminum capacitor and 470uF/63V polymer capacitor connect in parallel.

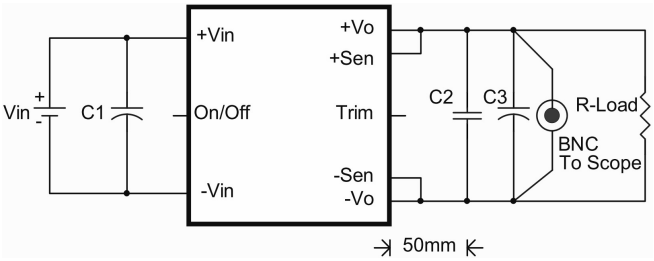
Cin:1000uF/100V (KMG) aluminum capacitor and 470uF/63V polymer capacitor connect in parallel.

7.2 Input Derating Curve

CFDHR500-24SXX series has Derating by Input Voltage is required shown below.



7.3 Output Ripple and Noise



C1:2200uF/63V ESR<0.056Ω

C2:1uF/1210 ceramic capacitor

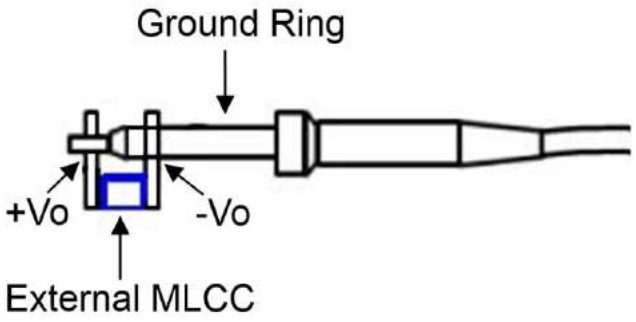
C3:10uF polymer tantalum capacitor (ESR ≦0.05Ω)

Output ripple and noise measured with 10uF polymer tantalum capacitor and 1uF ceramic capacitors across

output. A 20 MHz bandwidth oscilloscope is normally used for the measurement.

The conventional ground clip on an oscilloscope probe should never be used in this kind of measurement. This clip, when placed in a field of radiated high frequency energy,acts as an antenna or inductive pickup loop, creating an extraneous voltage that is not part of the output noise of the converter.

Another method is shown in below,in case of coaxial-cable/BNC is not available.The noise pickup is eliminated by pressing scope probe ground ring directly against the -Vout terminal while the tip contacts the +Vout terminal. This makes the shortest possible connection across the output terminals.



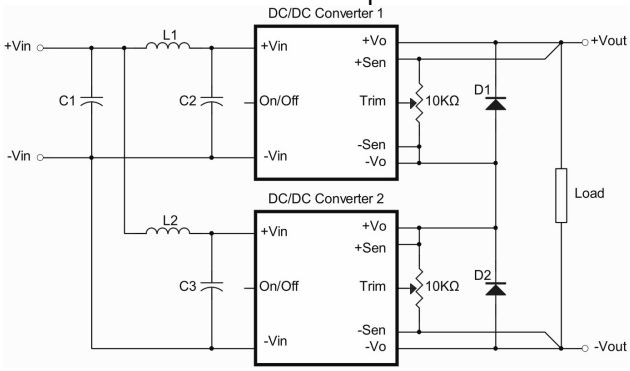
7.4 Output Capacitance

The CFDHR500-24SXX series converters provide unconditional stability with or without external capacitors. For good transient response,low ESR output capacitors should be located close to the point of load (<100mm). PCB design emphasizes low resistance and inductance tracks in consideration of high current applications. Output capacitors with their associated ESR values have an impact on loop stability and bandwidth. CHEWINS's converters are designed to work with load capacitance to see specifications.

8. Series and Parallel Operation

8.1 Series Operation

Series operation is possible by connecting the outputs two or more units.Connection is shown in below.The output current in series connection should be lower than the lowest rate current in each power module.



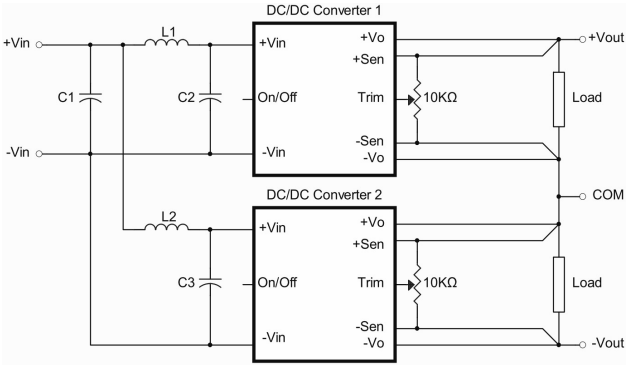
Simple Series Operation Connect Circuit

L1, L2:1.0uH
C1,C2,C3:2200uF/63V ESR<0.056Ω

Note:

1. If the impedance of input line is high,C1,C2,C3 capacitance must be more than above.Use more than two recommended capacitor above in parallel when ambient temperature becomes lower than -20℃.
2. Recommend Schottky diode (D1,D2) be connected across the output of each series connected converter, so that if one converter shuts down for any reason, then the output stage won't be thermally overstressed. Without this external diode, the output stage of the shut-down converter could carry the load current provided by the other series converters,with its MOSFETs conducting through the body diodes.The MOSFETs could then be overstressed and fail. The external diode should be capable of handling the full load current for as long as the application is expected to run with any unit shut down.

Series for ±output operation is possible by connecting the outputs two units, as shown in the schematic below.



Simple ±Output Operation Connect Circuit

L1, L2:1.0uH

C1,C2,C3: 2200uF/63V ESR<0.05Ω

Note:

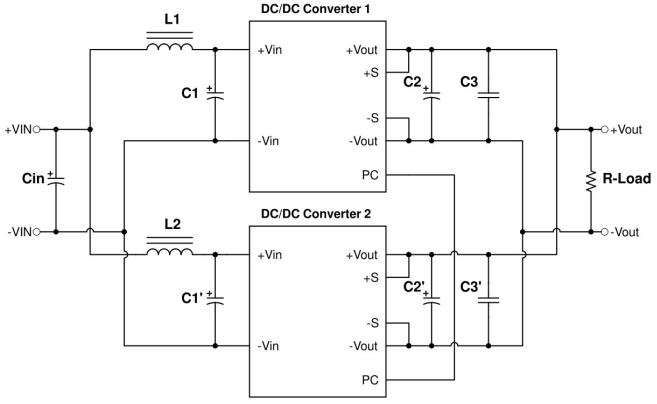
If the impedance of input line is high,C1,C2,C3 capacitance must be more than above. Use more than two recommended capacitor above in parallel when ambient temperature becomes lower than -20℃.

8.2 Parallel Operation

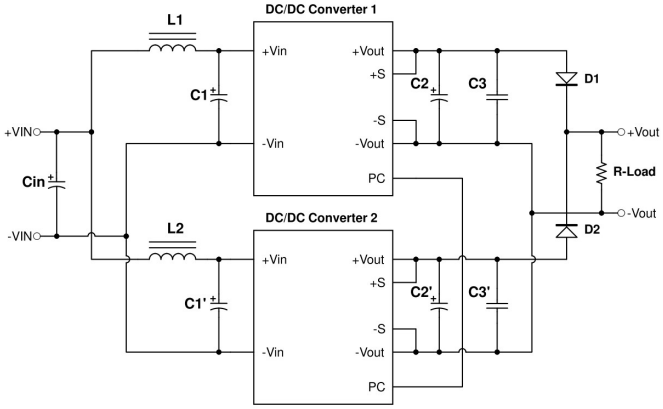
The CFDHR500-24SXX series are also designed for parallel operation. When paralleled, the load current can be equally shared between the modules by connecting the PC pins together.

There are two different parallel operations for CFDHR500-24SXX series,one is parallel operation when load can't be supplied by only one power unit; the other is the N+1 redundant operation which is high reliable for load of N units by using N+1 units.

(a) parallel operation



(b) N+1 redundant connection



L1,L2:1.0uH

Cin,C1,C1': 2200uF/63V ESR<0.056Ω

C2, C2':1000uF/63V

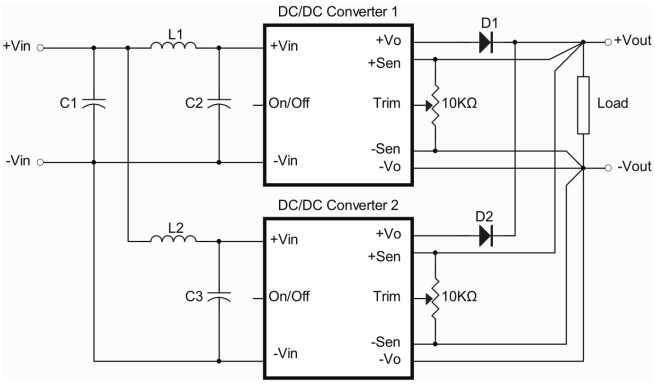
C3, C3':1uF MLCC

Note:

If the impedance of input line is high,Cin,C1 capacitance must be more than above.Use more than two recommended capacitor above in parallel when ambient temperature becomes lower than -20℃.

8.3 Redundant Operation

Parallel for redundancy operation is possible by connecting the units as shown in the schematic below.The current of each converter become unbalance by a slight difference of the output voltage.Make sure that the output voltage of units of equal value and the output current from each power supply does not exceed the rate current.Suggest use an external potentiometer to adjust output voltage from each power supply.



Simple Redundant Operation Connect Circuit

L1,L2:1.0uH

C1,C2,C3:2200uF/63V ESR<0.056Ω

Note:

If the impedance of input line is high, C1,C2,C3 capacitance must be more than above. Use more than two recommended capacitor above in parallel when ambient temperature becomes lower than -20℃.

9. Thermal Design

9.1 Operating Temperature Range

The CFDHR500-24SXX series converters can be operated within a wide case temperature range of -40℃ to 105℃. Consideration must be given to the derating curves when ascertaining maximum power that can be drawn from the converter. The maximum power drawn from open quarter brick models is influenced by usual factors, such as:

Input voltage range
Output load current
Forced air or natural convection
Heat sink optional

9.2 Convection Requirements for Cooling

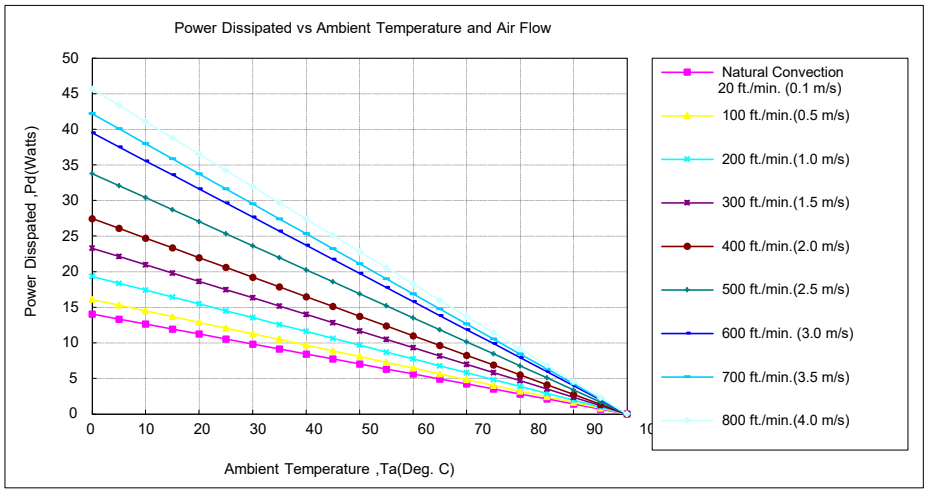
To predict the approximate cooling needed for the quarter brick module, refer to the power derating curves in section 9.4. These derating curves are approximations of the ambient temperatures and airflows required to keep the power module temperature below its maximum rating. Once the module is assembled in the actual system, the module's temperature should be monitored to ensure it does not exceed 105℃ as measured at the center of the top of the case (thus verifying proper cooling).

9.3 Thermal Considerations

The power module operates in a variety of thermal environments; however, sufficient cooling should be provided to help ensure reliable operation of the unit. Heat is removed by conduction, convection, and radiation to the surrounding environment. The example is presented in section 9.4 . The power output of the module should not be allowed to exceed rated power (V_{o_set} x I_{o_max}).

9.4 Power Derating

The operating case temperature range of FDHR500-24SXX series is -40℃ to +105℃.When operating the CFDHR500-24SXX series, proper derating or cooling is needed. The maximum case temperature under any operating condition should not exceed 105℃.
The following curve is the de-rating curve of CFDHR500-24SXX series without heat sink.



AIR FLOW RATE	TYPICAL Rca
Natural Convection 20ft./min.(0.1m/s)	7.12℃/W
100ft./min.(0.5m/s)	6.21℃/W
200 ft./min.(1.0m/s)	5.17℃/W
300 ft./min.(1.5m/s)	4.29℃/W
400 ft./min.(2.0m/s)	3.64℃/W
500 ft./min.(2.5m/s)	2.96℃/W
600 ft./min.(2.5m/s)	2.53℃/W
700 ft./min.(2.5m/s)	2.37℃/W
800 ft./min.(2.5m/s)	2.19℃/W

Example:

What is the minimum airflow necessary for a CFDHR500-24S24 operating at nominal line voltage,an 70% Load output current of 14.6A, and a maximum ambient temperature of 25℃

Solution:

Given:V_{in}= 24V_{DC},Vo= 24V_{DC}, I_o= 14.6A

Determine Power dissipation (P_d): P_d= P_i-P_o= P_o(1-η)/η, P_d= 24×14.6×(1-0.91)/0.91= 34.65Watts

Determine airflow:Given: P_d= 34.65W and T_a= 25℃

Check Power Derating curve: Minimum airflow= 800 ft./min.

Verify:

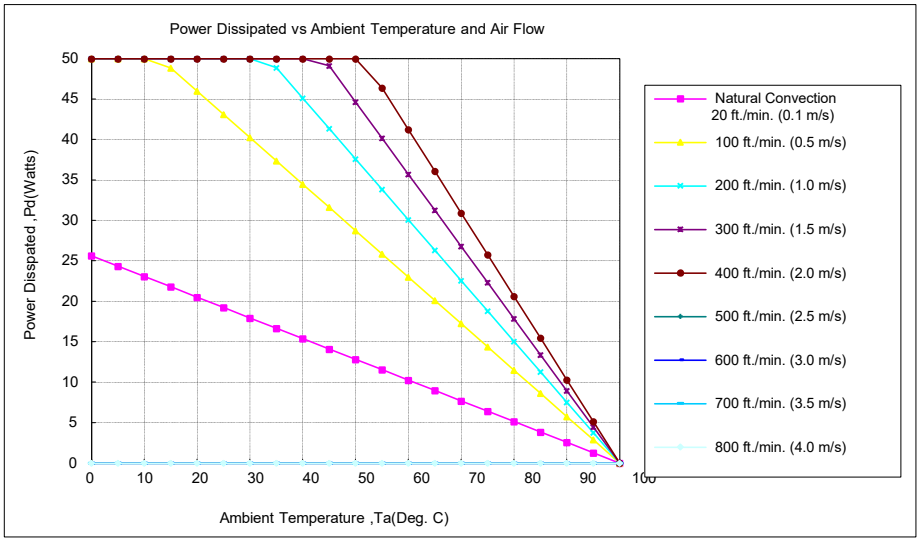
Maximum temperature rise is $\Delta T = P_d \times R_{ca}$ = 34.65×2.19= 75.88℃

Maximum case temperature is $T_c = T_a + \Delta T$= 100.9℃<105℃

Where:

The R_{ca} is thermal resistance from case to ambient environment.

T_a is ambient temperature and T_c is case temperature.



AIR FLOW RATE	TYPICAL R_{ca}
Natural Convection 20ft./min. (0.1m/s)	3.9 ℃/W
100 ft./min. (0.5m/s)	1.74 ℃/W
200 ft./min. (1.0m/s)	1.33 ℃/W
300 ft./min. (1.5m/s)	1.12 ℃/W
400 ft./min. (2.0m/s)	0.97 ℃/W

Example with heatsink HBL210 (M-C308):

What is the minimum airflow necessary for a CFDHR500-24S24 operating at nominal line voltage,an output current of 21A,and a maximum ambient temperature of 55℃

Solution:

Given:Vin= 24V_{DC},Vo= 24V_{DC},Io= 21A

Determine Power dissipation (P_d):P_d= Pi-Po= Po(1-η)/η,P_d= 24×21×(1-0.91)/0.91=49.85Watts

Determine airflow:Given:P_d= 49.85W and T_a = 55℃

Check above Power de-rating curve:Minimum airflow= 400 ft./min

Verify:

Maximum temperature rise is $\Delta T = P_d \times R_{ca}$= 49.85×0.97= 48.35℃

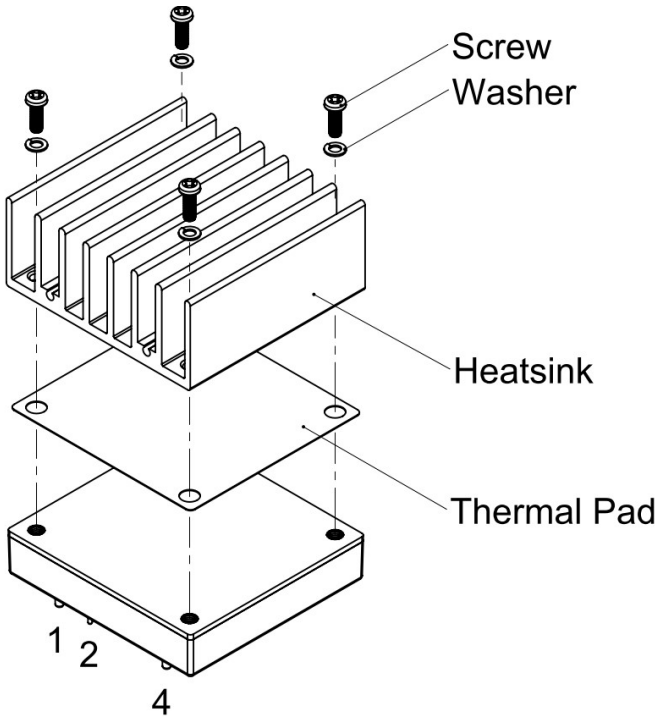
Maximum case temperature is $T_c = T_a + \Delta T$= 103.35℃<105℃

Where:

The R_{ca} is thermal resistance from case to ambient environment.

T_a is ambient temperature and T_c is case temperature.

9.5 Half Brick Heat Sinks:

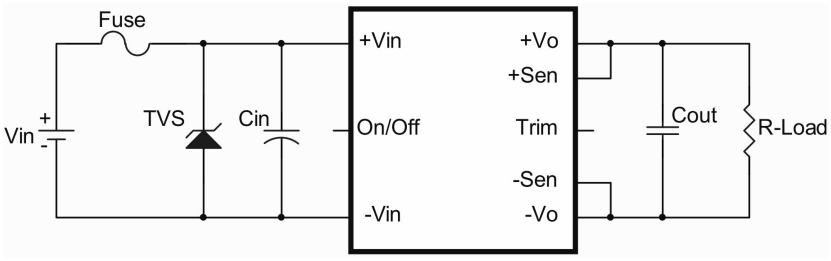


THERMAL PAD PH01: SZ 56.9*60*0.25 mm (G6135041091)
SCREW K308W: SMP+SW M3*8L (G75A1300322)

10. Safety/EMC

10.1 Input Fusing and Safety Considerations

The CFDHR500-24SXX series converters have no internal fuse. In order to achieve maximum safety and system protection, always use an input line fuse. We recommended a 80A time delay fuse for all models. It is recommended that the circuit have a transient voltage suppressor diode (TVS) across the input terminal to protect the unit against surge or spike voltage and input reverse voltage (as shown).



The external input capacitor (Cin) and transient voltage suppressor diode (TVS) are required if CFDHR500-24SXX series has to meet EN61000-4-4, EN61000-4-5.
The Cin recommended a 2200uF/63V (Nichicon PW series) aluminum capacitor. And the TVS recommended a SMDJ40A transient voltage suppressor.

10.2 EMC Considerations

EMI Test standard: EN55032 Class A / EN50121-3-2:2016 Conducted & Radiated Emission
Test Condition: Input Voltage: 24Vdc, Output Load: Full Load

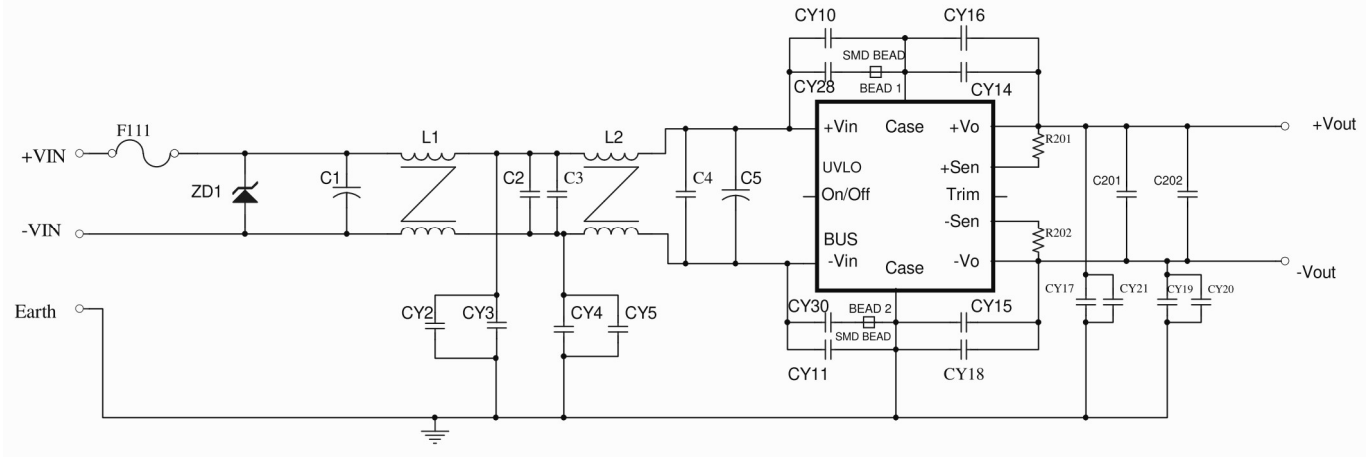


Figure1 Connection circuit

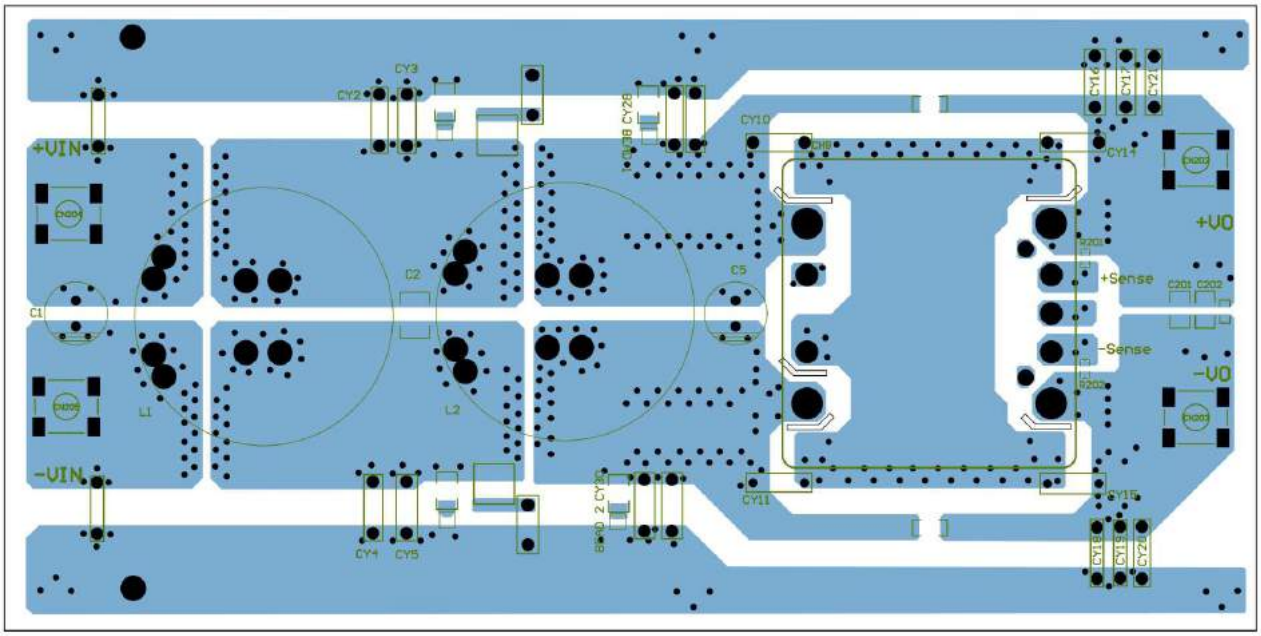


Figure2 PCB layout top view

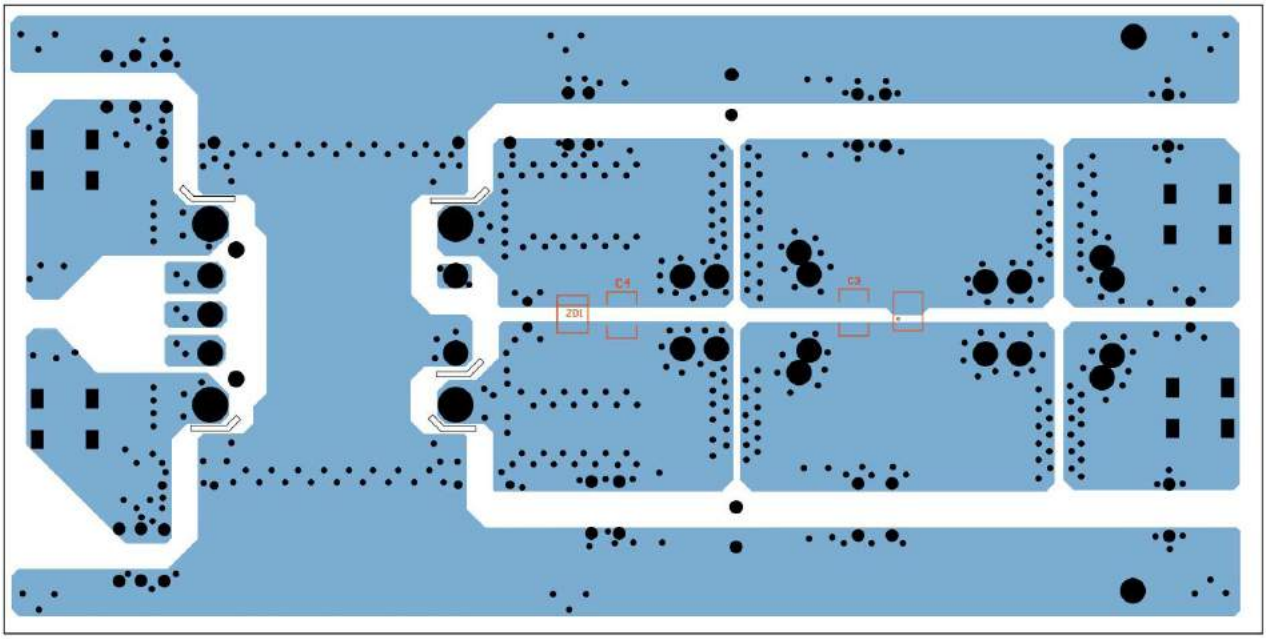


Figure3 PCB layout bottom view

Components value:

	Model Number				
Model Name	24S12	24S24	24S28	24S48	24S54
C1, C5	820uF/50V				
C2	10uF/50V				
C3, C4	NC				10uF/50V
C201	10uF/50V				4.7uF/50V
C202	1uF/250V SMD 1812				
CY2, CY4	1000pF/400V DIP				
CY3, CY5, CY10, CY11, CY16, CY17, CY18, CY19	4700pF/250V DIP				
CY20, CY21	NC				4700pF/250V DIP
CY14, CY15	2200pF/400V DIP				
BEAD 1, BEAD 2	BPH 4030225-400T-G				
CY28, CY30	SMD 2200pF/250V$_{AC}$				
R201, R202	0R 1%				
ZD1	SMDJ40A				
L1, L2	1.58mH				

Note:

C1,C5:Chimei con KZN aluminum capacitor or equivalent.
C2,C3,C4: 2220 X7R eramic.
C201,C202: 1812 X7R eramic.
C4,C5: Suscon aluminum capacitor or equivalent.
CY2,CY4: TDK Y1 capacitor or equivalent.
CY14,CY15: TDK Y1 capacitor or equivalent.
CY3,CY5,CY10,CY11,CY16,CY17,CY18,CY19: TDK Y1 capacitor or equivalent.
CY20,CY21: TDK Y1 capacitor or equivalent.
CY28,CY30: Y2 CAP. SMD 2211 X7R.
BEAD 1,BEAD 2: SMD bead core TAI-TECH or equivalent.
R201,R202: CHIP RESISTOR 0805.
ZD1: TVS SMD DO-214AB LITTLEFUSE.
L1,L2: 2.0mm*2/3.5T Nanocrystalline W424 VAC or equivalent.

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